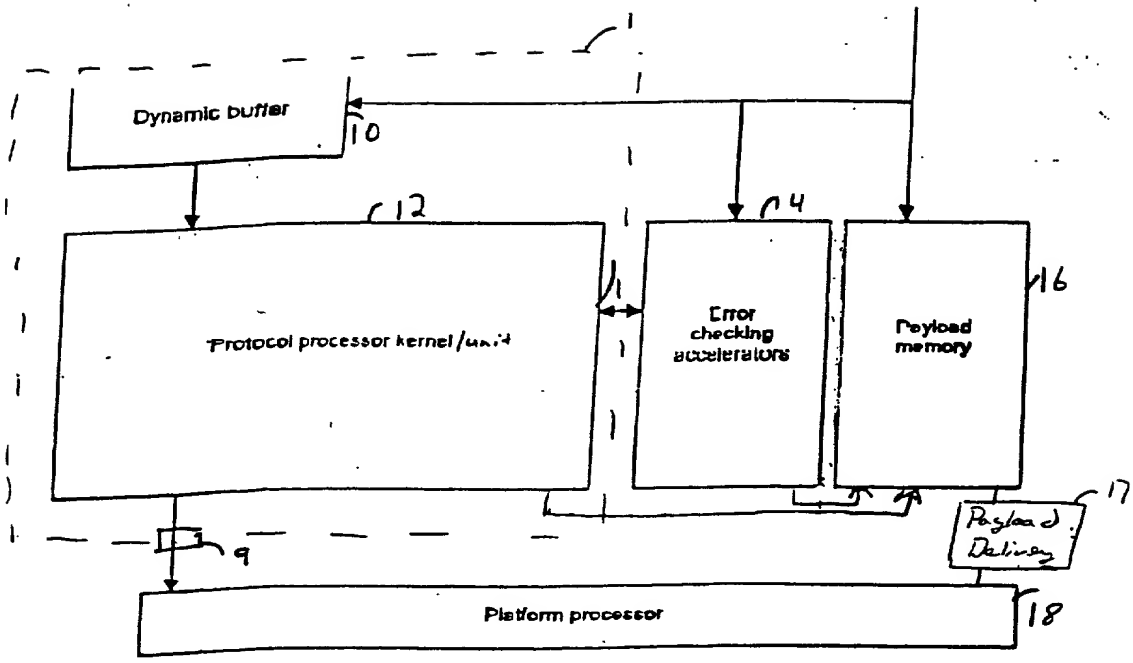

1
Dynamic buffer
10
12
14
Protocol processor kernel/unit
Error checking accelerators
Payload memory
16
17
Payload Delivery
9
Platform processor
18

Figure 1

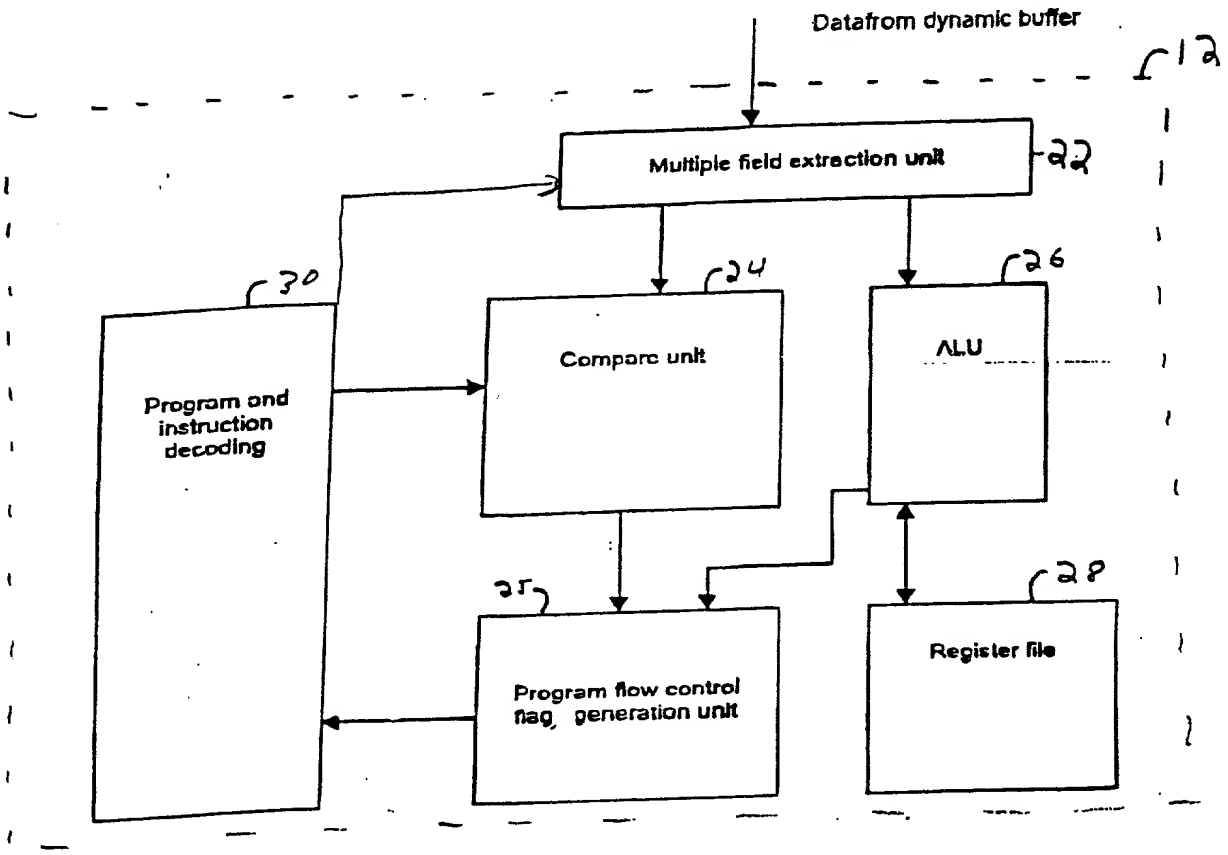

Data from dynamic buffer
12
Multiple field extraction unit
22
30
24
26
Program and instruction decoding
Compare unit
ALU
25
28
Program flow control flag generation unit
Register file

Figure 2

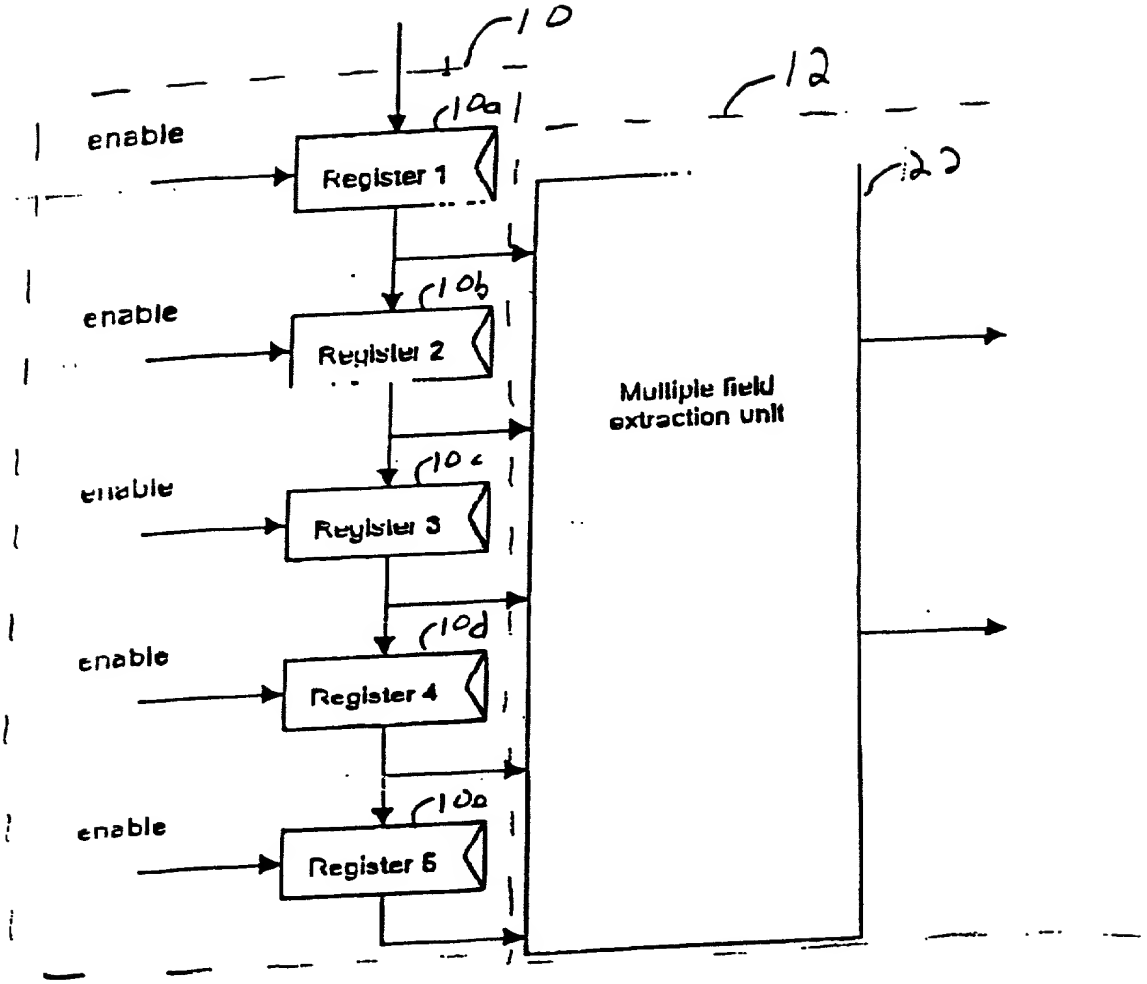

10
12
10a
enable
Register 1
22
10b
enable
Register 2
Multiple field extraction unit
10c
enable
Register 3
10d
enable
Register 4
10e
enable
Register 5

Figura 3

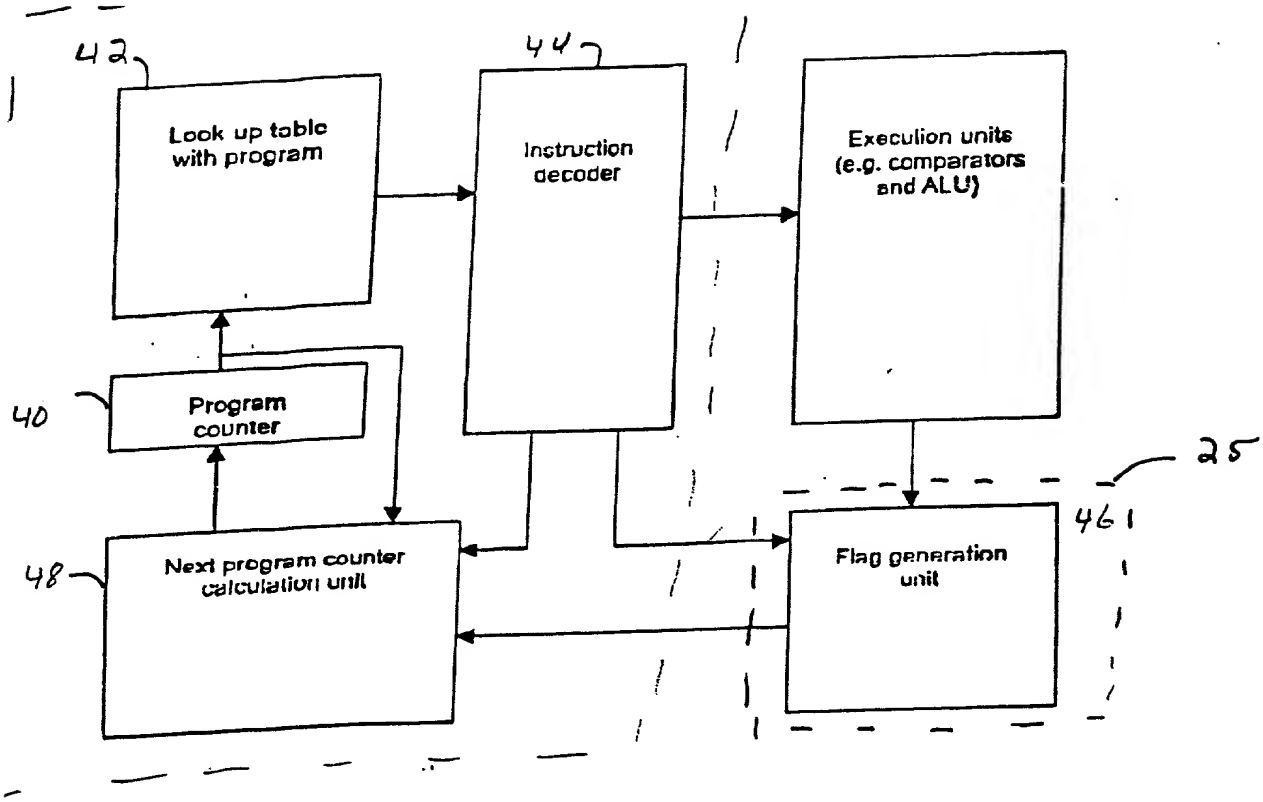

42
Look up table with program
44
Instruction decoder
Execution units (e.g. comparators and ALU)
40
Program counter
25
46
Flag generation unit
48
Next program counter calculation unit

Figure 4

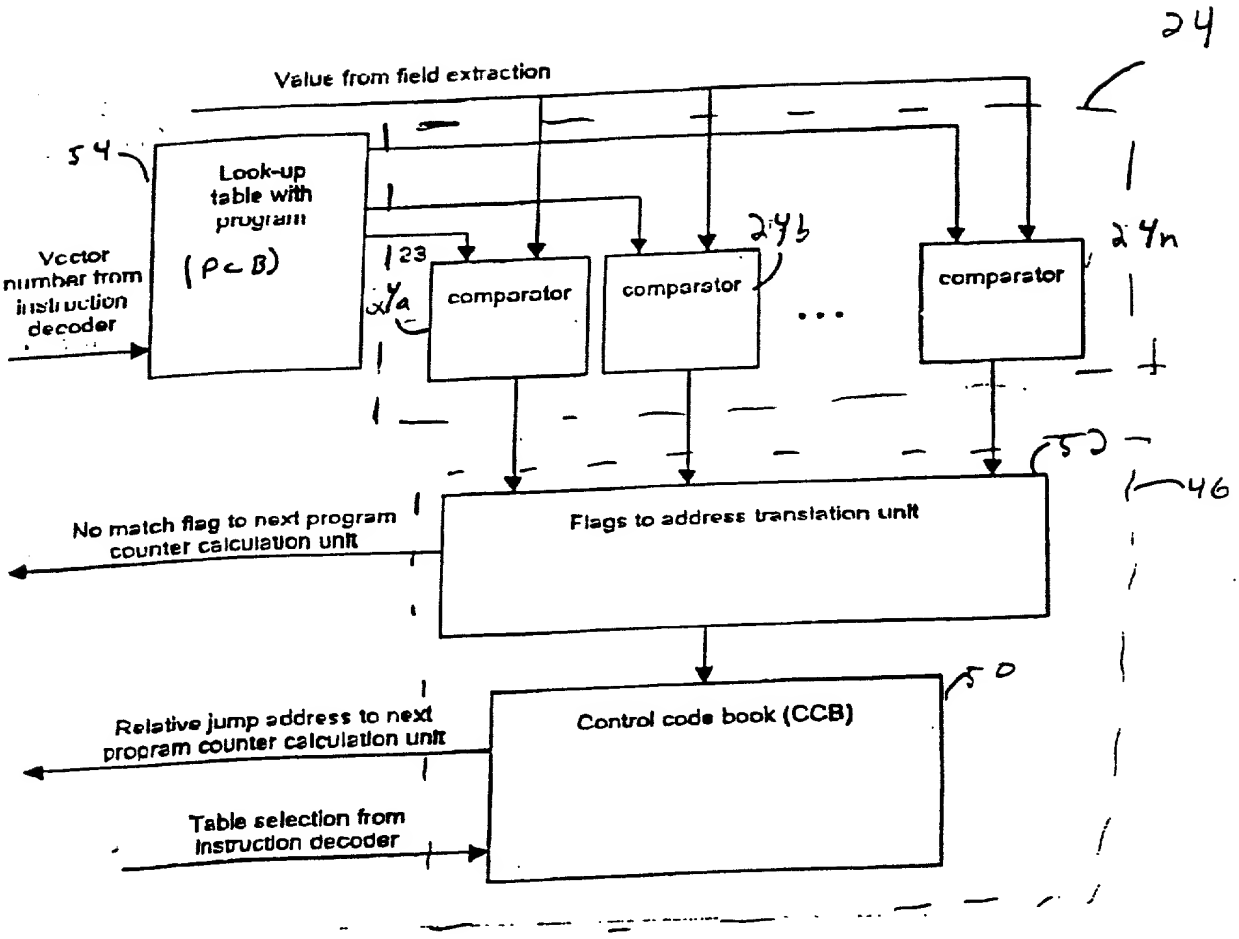

24
Value from field extraction
54
Look-up table with program
(PCB)
Vector number from instruction decoder
123
comparator
comparator
comparator
24b
24n
52
46
No match flag to next program counter calculation unit
Flags to address translation unit
50
Relative jump address to next program counter calculation unit
Control code book (CCB)
Table selection from instruction decoder

Figure 5

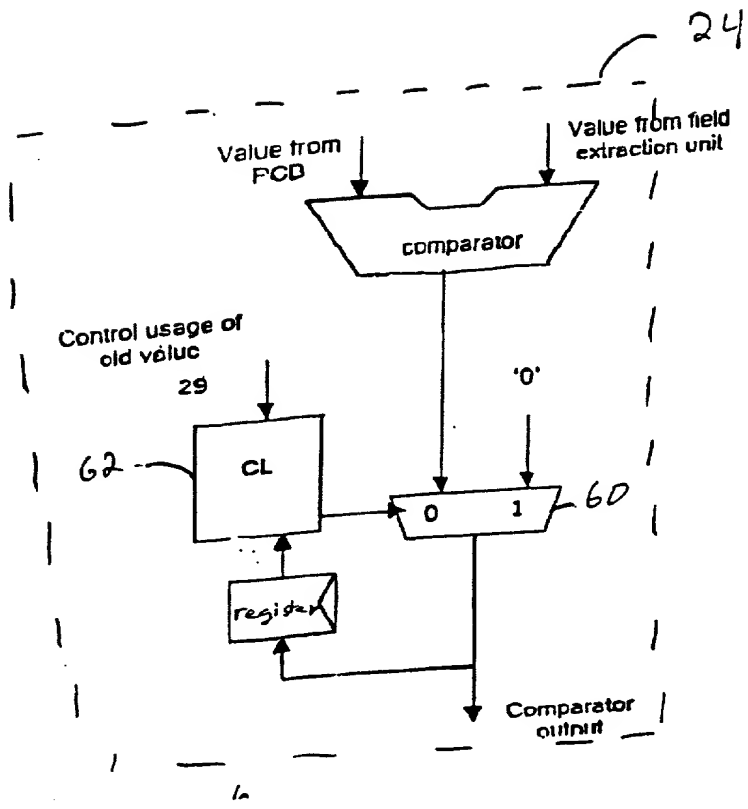


Figure 6

The combinational logic (CL) Block

(29)	(31)	(32)
0	0	0
0	1	0
1	0	1
1	1	0

Figure 6B

Figure 7

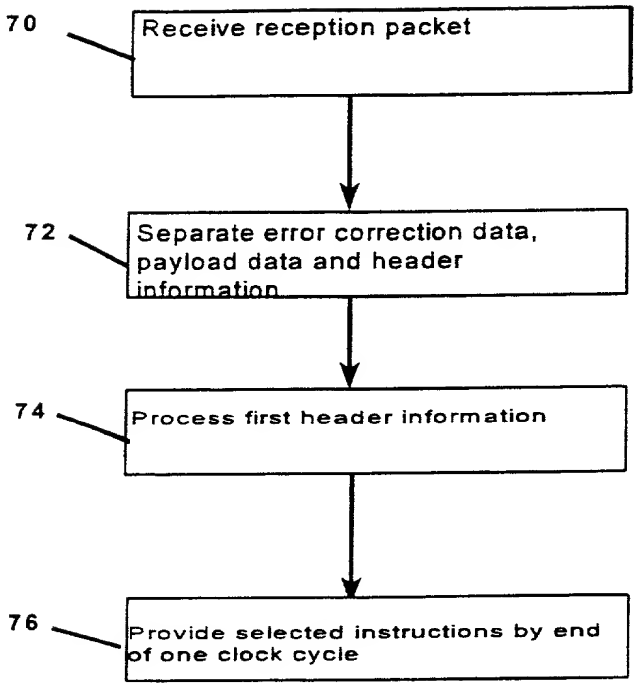

70
Receive reception packet
72
Separate error correction data, payload data and header information
74
Process first header information
76
Provide selected instructions by end of one clock cycle

Figure 8

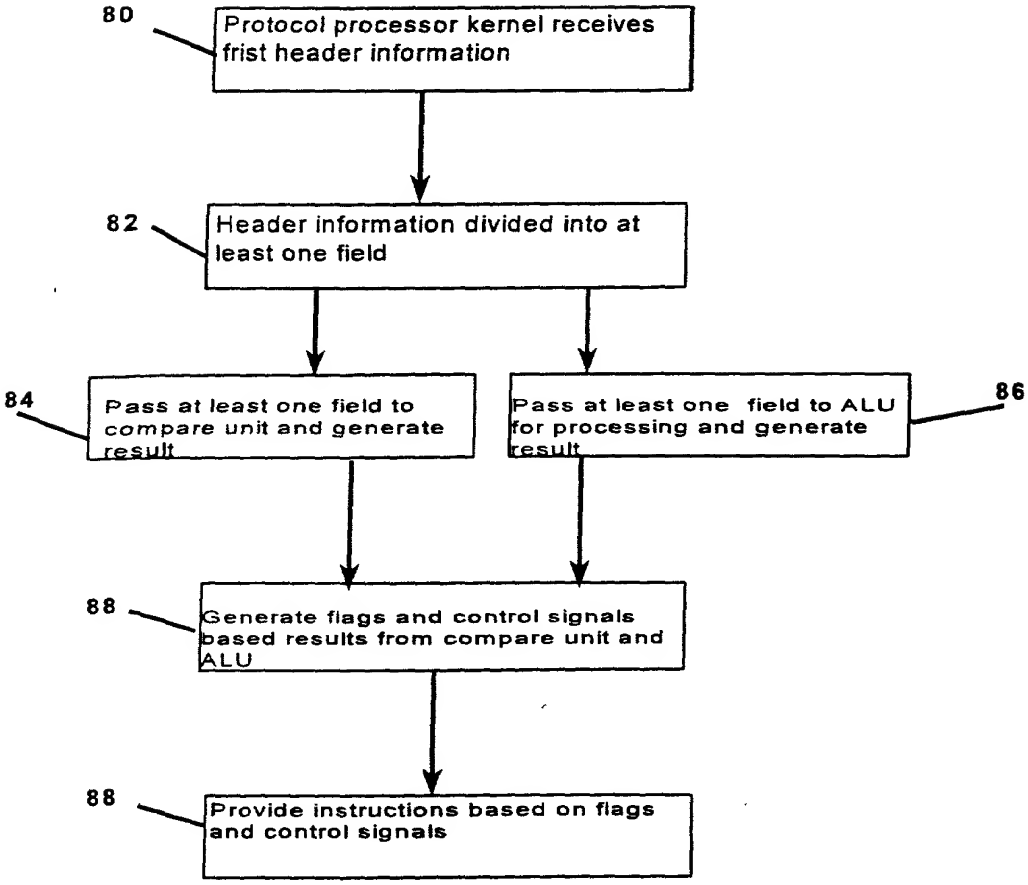
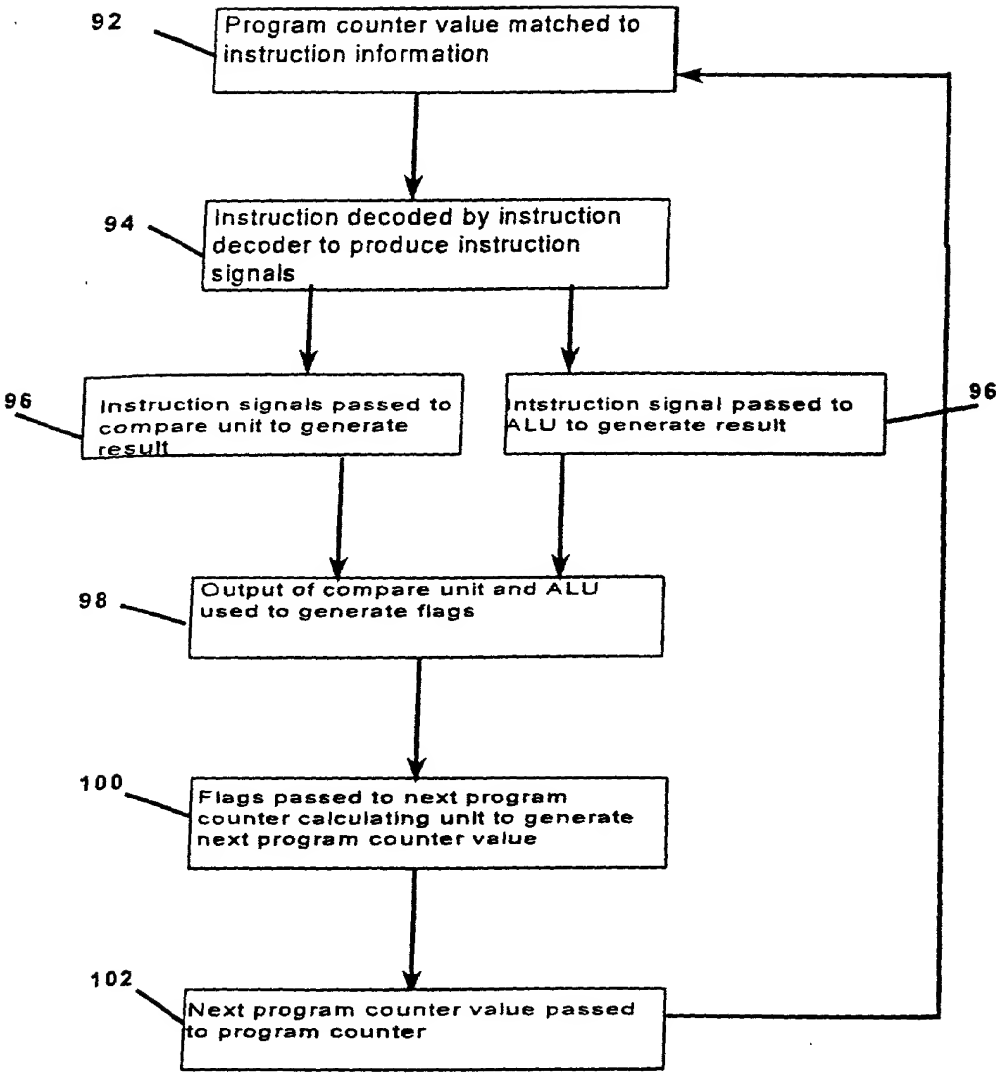

80
Protocol processor kernel receives frist header information
82
Header information divided into at least one field
84
Pass at least one field to compare unit and generate result
86
Pass at least one field to ALU for processing and generate result
88
Generate flags and control signals based results from compare unit and ALU
88
Provide instructions based on flags and control signals

Figure 9


92
Program counter value matched to instruction information
94
Instruction decoded by instruction decoder to produce instruction signals
96
Instruction signals passed to compare unit to generate result
Intstruction signal passed to ALU to generate result
96
98
Output of compare unit and ALU used to generate flags
100
Flags passed to next program counter calculating unit to generate next program counter value
102
Next program counter value passed to program counter

Frg. 10

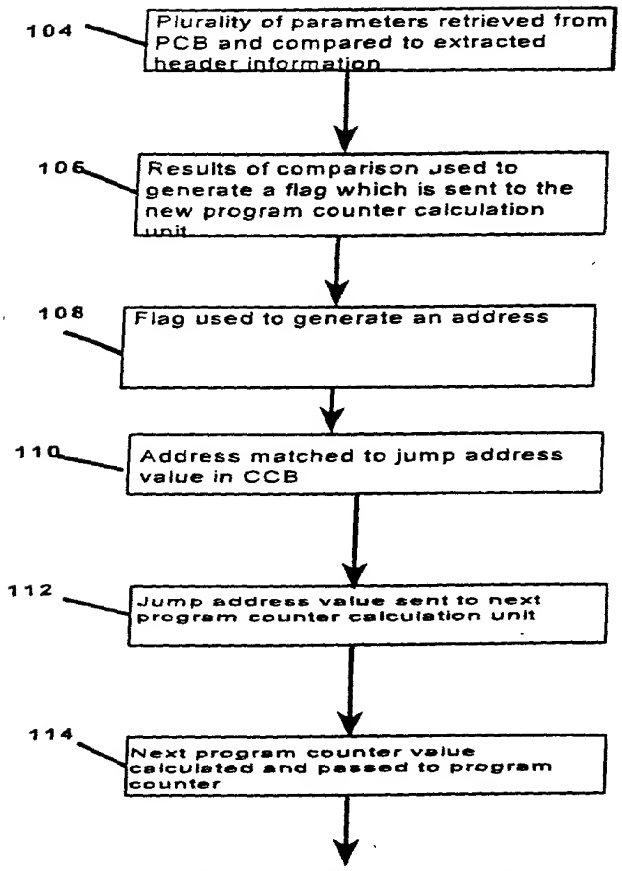


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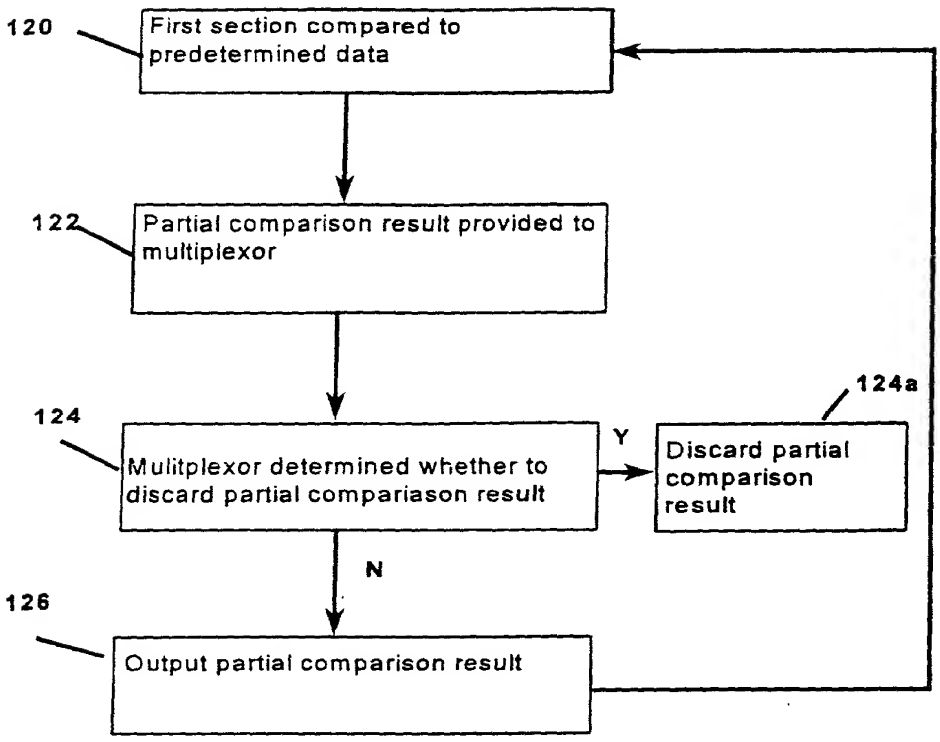
Figure 11


120
First section compared to predetermined data
122
Partial comparison result provided to multiplexor
124
Mulitplexor determined whether to discard partial compariason result
Y
124a
Discard partial comparison result
N
126
Output partial comparison result